

U.S. Patent Appln. No.: 10/052,779  
Amendment dated: November 17, 2003  
Reply to Office Action of July 22, 2003

### REMARKS

The Office Action dated July 22, 2003 has been carefully reviewed, and these remarks respond to that Office Action. Applicant respectfully requests reconsideration of the application, as amended, and allowance of this application.

Applicant acknowledges, with appreciation, the Office's indication that claims 9-11 and 17 in this application contain patentable subject matter.

Upon entry of this Amendment, claims 9-11, 17, 19, and 21 will remain pending in this application. Claims 1, 3-8, 12-16, 18, and 20 previously were canceled from this application. Claims 2 and 22 are currently canceled. Applicant has amended claims 19 and 21 through this Amendment, as described above. No new matter is included in this Amendment, and no additional claim fees are due as a result of this Amendment.

### Objection to the Drawings

Applicant has amended Figure 6 as suggested by the Examiner.

Applicant requests the Examiner to withdraw the objection to the drawings.

### Rejection Under 35 U.S.C. § 112, First Paragraph

The Examiner rejects claims 19 and 21 under 35 U.S.C. § 112, first paragraph. Applicant traverses.

The Examiner refers to Figures 4 and 6 and references elements 111, 115, and others and that they need to be recited in some form in claims 19 and 21.

Claims 19 and 21 do not relate to Figures 4 and 6. Rather, they relate to Figures 15, 16, and 18. Figure 4 relates to a current mirror circuit. Claim 19 relates to a current source circuit. Applicant cites to the description of Figures 15 and 16.

“When the voltage  $V_{d1}$  decreases, then the voltages ( $V_{g1} V_{d1}$ ), ( $V_{g1} 2V_{d1}$ ), . . . , ( $V_{g1} nV_{d1}$ ) increase respectively. And also the current that flows through NMOS transistors  $215_1, 215_2, \dots, 215_n$  increases respectively. Because of the compensation of the decrease, the sum total of the current which flows through NMOS transistors  $215_0, 215_1, 215_2, \dots, 215_n$  can nearly be made

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constant. Therefore, the constant current region becomes extended under conditions of lower supply voltage, and the characteristics of constant current source can be improved even if the semiconductor circuit operates in a low supply voltage." See paragraph 69.

Importantly, there is no NMOS transistor 111 or current source 115 in Figure 16. Accordingly, because support in the specification is found based on a different Figure, Applicant submits claim 19 is allowable over the 112, first paragraph, rejection. See also the related description of Figure 15.

Regarding claim 21, the examiner alleges that claim 21 does not include the elements 115, 121 and 122 of Figure 4. Again, Applicant submits that Figure 4 relates to a current mirror circuit while claim 21 relates to a current source circuit as described in Figure 18. There is no NMOS transistor 111 or current source 115 in the Fig. 18.

**Rejection Under 35 U.S.C. § 112, Second Paragraph**

Applicant has amended the first occurrence of "node" in claim 19 to read "voltage circuit" as suggested by the Examiner.

Claim 21 has been amended as well to clarify the invention.

**Rejection of Claims 2 and 22**

Claims 2 and 22 stand rejected over art. These claims are currently cancelled. The rejection has been overcome.

As all rejections and objections have been addressed, the application is believed to be in condition for allowance.


If any additional claim fees are due along with this paper, the Commissioner is authorized to debit our Deposit Account No. 19-0733 to cover any necessary fees. Also, if an extension of time is needed that is not accounted for in this Amendment or any accompanying papers filed with it, the necessary extension is requested. Please charge the extension fee to Deposit Account No. 19-0733.

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All rejections having been addressed, Applicant respectfully submits that this application is in condition for immediate allowance and respectfully solicits prompt notification of the same.

Respectfully submitted,

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